

IN THE CLAIMS

Claims 1-25 (Canceled).

26 (Previously Presented). A semiconductor structure, comprising:
a support;
a first material deposited on said support, said first material being a dielectric having a first etch rate;
a trench formed through said first material and into the support; and
a trench filler material deposited in the trench, the trench filler material having an etch rate that is less than 1.2 times the first etch rate and substantially similar to or less than the first etch rate, the semiconductor structure having a planar exposed upper surface formed of said first material and said trench filler material.

27 (Original). The semiconductor device of claim 26, wherein the first material includes silicon dioxide deposited from tetraethylorthosilicate or a silane and oxygen system.

28 (Original). The semiconductor device of claim 26, wherein the first material includes silicon dioxide deposited by chemical vapor deposition.

29 (Original). The semiconductor device of claim 26, wherein the trench filler material includes silicon dioxide deposited from tetraethylorthosilicate or a silane and oxygen system.

30 (Original). The semiconductor device of claim 26, wherein the trench filler material includes silicon dioxide deposited by chemical vapor deposition.

Claims 31-35 (Canceled).